

PRODUCT/PROCESS CHANGE NOTIFICATION PCN12439 – Additional information

AMKOR (Taiwan) Additional DPS line for WLCSP 12" STM32L4x, STM32L5x, STM32G0x, STM32G4x listed products

MDG - Microcontrollers Division (MCD)

What are the changes?

Changes described in table below:

	Current	Current source		
RDL Site	ASE Kaohsiung	ASE Kaohsiung Amko		
(Wafer Level Processing)	Taiwan WLCSP12" Taiwan WLCSP12"		/LCSP12"	
DPS Site	ASE Kaohsiung	Amkor T3	Amkor T6	
(Die Processing Services)	Taiwan WLCSP12"	Taiwan WLCSP12"	Taiwan WLCSP12"	

How can the change be seen?

No change in Form, Fit or Function

How to order samples? *

For all samples request linked to this PCN, please:

- place a <u>Non-standard</u> sample order (choose Sample Non Std Type from pull down menu)
- insert the PCN number "PCN 12439" into the NPO Electronic Sheet/Regional Sheet
- request sample(s) through Notice tool, indicating a single Commercial Product for each request

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PO Nr.	Carrier Code: 0001 Price Policy: 05 Currency: 02 V.S. DOLLAR · Reg Name:	
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Reliability Evaluation Report MDG-MCD-RER2101

AMKOR (Taiwan) Additional DPS line for WLCSP 12" STM32L4x, STM32L5x, STM32G0x, STM32G4x products

PCN12439

Genera	I Information for TV		Traceability
Commercial Product	: STM32F476MGY6TR	Diffusion Plant	: TSMC Fab14
Product Line	: 415X66	Assembly Plant	: Amkor ATT1 (Bumping) Amkor ATT6 (DPS)
Die revision	: X415CCC4		
Package	: WLCSP 81L	Reliability Assessment	
Silicon Technology	: 90nm eFlash Generic TSMC	Pass	
Division	: MDG-MCD	Fail	
Reliability Maturity Level	: 30	Investigation required	

Note: this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).

Version	Date	Author	Function
1.0	15 th Oct 2021	Céline Navarro	MDG-MCD Q&R Technicien

APPROVED BY:

Function	Location	Name	Date
Division Quality Manager	RSST	Pascal NARCHE	15th Oct 2021
Back-end MCD Quality Manager	RSST	Gisele SEUBE	15 th Oct 2021



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1 RELIABILITY EVALUATION OVERVIEW

1.1 **Objective**

The aim of this report is to present results of the reliability evaluation on WLCSP12" Test Vehicle with DPS (Die Processing Services for device singulation and packing in Tape & Reel) in ATT6 site.

This Production Change Notification (PCN12439) concerns AMKOR (Taiwan) Additional DPS line for WLCSP 12" STM32L4x, STM32L5x, STM32G0x, STM32G4x products.

Changes are described here below:

	Current	t source	Added site	
RDL Site	ASE Kaohsiung	Amk	kor T1	
(Wafer Level Processing)	Taiwan WLCSP12"	Taiwan W	/LCSP12"	
DPS Site	ASE Kaohsiung	Amkor T3	Amkor T6	
(Die Processing Services)	Taiwan WLCSP12"	Taiwan WLCSP12"	Taiwan WLCSP12"	

1.2 Reliability Strategy

Test vehicle is described here below:

Product	Process or Package	Assembly plant
STM32F476MGY6TR	WLCSP 81L	AMKOR ATT1 (Bumping) AMKOR ATT6 (DPS)

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard.

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for AMKOR (Taiwan) Additional DPS line for WLCSP 12" STM32L4x, STM32L5x, STM32G0x, STM32G4x products.

Refer to Section 3.0 for reliability test results.



2 TEST VEHICLE CHARACTERISTICS

2.1 **Description**

Package	Bumping Line	Package	Device	Diffusion	Number
line	DPS line		(RawLine)	Process	of Lots
WLCSP	AMKOR ATT1 AMKOR ATT6	WLCSP 81L	STM32F476 (00AQ*415ESC4)	TSMC90	3

2.2 Wafer fab information

<u>Table 1</u>

Wafer fab information		
FAB1		
Wafer fab name / location	Fab14 TSMC TAIWAN	
Wafer diameter (inches)	12	
Wafer thickness (µm)	775µm +/- 25µm	
Silicon process technology	TSMC 90nm eFlash Generic	
Number of masks	45	
Die finishing front side (passivation)	PSG + NITRIDE	
materials/thicknesses		
Die finishing back side		
Materials/thicknesses		
Die area (Stepping die size)	3794.4 x 4443.4 μm	
Die pad size	123, 59	
Sawing street width (X,Y) (µm)	80, 80	
	Metal 1 TaN/Ta/CuSeed/Cu 0.240 µm	
	Metal 2 TaN/Ta/CuSeed/Cu 0.310 µm	
	Metal 3 TaN/Ta/CuSeed/Cu 0.310 µm	
Metal levels/Materials/Thicknesses	Metal 4 TaN/Ta/CuSeed/Cu 0.310 µm	
	Metal 5 TaN/Ta/CuSeed/Cu 0.310 µm	
	Metal 6 TaN/Ta/CuSeed/Cu 0.850 µm	
	Metal 7 AlCu 1.450 µm	



2.3 Assembly information

<u>Table 2</u>

Assembly Information	
Package 1 - WLCSP81L die 415	
Assembly plant name / location	AMKOR ATT1 (Bumping) & ATT6 (DPS) / KOREA
Pitch (mm)	0.4
Die thickness after back-grinding (µm)	355µm +/-10µm
Die sawing method	Laser Groove + Step cut mechanical
Bill of Material elements	
Balls metallurgy/diameter	Solder ball SACN125 Diam 230um
Routing/Redistribution layer (RDL) material (CSP)	RDL Copper
Passivation material (CSP)	PBO passivation HD8820
Backside coating material/thickness (CSP)	Back side coating PET film 25µm
Package Moisture Sensitivity Level	1
(JEDEC J-STD020D)	



2.4 Reliability testing information

<u>Table 3</u>

Reliability Testing Information	
Reliability laboratory name / location	ST Grenoble / France

<u>Note:</u> ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs. ST certification document can be downloaded under the following link: <u>http://www.st.com/content/st_com/en/support/guality-and-reliability/certifications.html</u>

3 TESTS RESULTS SUMMARY

3.1 Lot information

Table 4

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	
1	9R037010 Wafer 01	Cut 1.3	A5102017	00AQ*415ESC4	WLCSP 81L	
2	9R037010 Wafer 02	Cut 1.3	A5102017	00AQ*415ESC4	WLCSP 81L	
3	9R037010 Wafer 03	Cut 1.3	A5102017	00AQ*415ESC4	WLCSP 81L	



3.2 Test plan and results summary

Table 5	- ACCELERATED	ENVIRONMENT	STRESS TESTS
I GOIG D			OTICEOU TEUTO

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
PC	J-STD-020	24h bake@125°C, MSL1 (168h@85C/85%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	3	308	924	Lot1: 0/308 Lot2: 0/308 Lot3: 0/308	
тс	JESD22-A104	Ta=−65/150°C Duration= 500cyc ⊠ After PC	3	77	231	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77	
UHAST	JESD22-A118	Ta=130°C ,85% RH Duration= 96hrs ⊠ After PC	3	77	231	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77	
HTSL	JESD 22-A103	Ta=150°C, Duration= 1000hrs ⊠ After PC	3	77	231	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77	
ТНВ	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 Duration= 1000hrs ⊠ After PC	3	77	231	Lot 1: 0/77 Lot 2: 0/77 Lot 3: 0/77	

Note: Test method revision reference is the one active at the date of reliability trial execution

Table 6 – PACKAGE ASSEMBLY INTEGRITY TESTS

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
СА	Construction Analysis including -Physical dimensions	Internal ST specs JESD22-B100	3	50	150	Lot1: 0/50 Lot2 : 0/50 Lot3 : 0/50	No concern TPY MDG CA_21_00015 lot1 TPY MDG CA_21_00015 lot2 TPY MDG CA_21_00015 lot3



4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
JESD22-B100	Physical Dimension
DMS 0061692	Reliability Tests and Criteria for Product Qualification
JESD22-A108	Temperature, Bias and Operating Life
JESD22-A103	High Temperature Storage Life
J-STD-020	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A101	Steady State Temperature Humidity Bias Life Test
JESD22-A113	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104	Temperature cycling
JESD22-A110	Temperature Humidity Bake

5 GLOSSARY

Reference	Short description
PC	Preconditioning (solder simulation)
ТНВ	Temperature Humidity Bias
тс	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
CA	Construction Analysis

6 REVISION HISTORY

Pavision	Author	Content	Approval List					
REVISION	Aution	description	Function	Location	Name	Date		
1.0	Céline Navarro	Initial release	Division Quality Managor	рсст	Pascal	15 th Oct		
			Division Quanty Manager	1221	NARCHE	2021		
			Back-end MCD Quality	RSST	Gisele SEUBE	15 th Oct		
			Manager			2021		



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